

**VLIW COMPUTER PROCESSING ARCHITECTURE HAVING THE PROGRAM
COUNTER STORED IN A REGISTER FILE REGISTER**

ABSTRACT OF THE DISCLOSURE

According to the invention, a processing core (12) comprising a processing
5 pipeline (100) having N-number of processing paths (56), each of which process instructions
(54) on M-bit data words. In addition, the processing core (12) includes one or more register
files (60), each preferably having Q-number of registers which are M-bits wide. Preferably,
one of the Q-number of registers in at least one of the register files (60) is a program counter
register dedicated to hold a program counter, and one of the Q-number of registers in at least
10 one of the register files is a zero register dedicated to hold a zero value. In this manner,
program jumps can be executed by adding values to the program counter in the program
counter register, and memory address values can be calculated by adding values to the
program counter stored in the program counter register or to the zero value stored in the zero
register.

15
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